A Miniature Ka-Band SMD Isolator for Space Application

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***Abstract*—In this paper, Cobham presents the development, manufacturing, and evaluation steps of a Ka-band SMD isolator according to ESA specification and requirements in the standard frequency range (17.7-20.2 GHz). Three configurations are proposed. A low power version based with a BeO 5 W chip load. A very low power version with an integrated absorber load, and a high power version with a BeO 10W chip load.**

***Index Terms*—Isolator, SMD, Ferrites, ESA, chip load, absorber, shielding.**

I. INTRODUCTION

ISOLATORS are still very important microwave components in modern telecommunication systems. Isolators are used to protect the transmission equipment, especially amplifiers, from parasitic radiations or impedance mismatch.

A breakthrough in antenna technology occurred in the 1960s with the introduction of passive and active phased arrays, and started to widely diffuse in the 1990s for defense applications mainly.

Whereas a traditional radar system integrates a transmitter, a feeder, and a parabolic dish mechanically steered; an active electronically scanned array (AESA) is composed of hundreds of transmit and receive (T/R) modules. T/R modules can be phase shifted independently to form groups of modules, which illuminates different areas, and offer a multiple-beam capability to the system.

The RF design of an AESA is different from traditional single beam systems in which one path conveys all the power to the antenna feeder.

The RF channels of an AESA system are composed of small integrated components, each handling a small fraction of total power. In this configuration, circulators are used as diplexers between transmit and receive paths.

In addition, the isolators protect the amplifiers of each transmit module (Figure 1), and also provide good impedance matching and isolation anywhere it is needed between two RF functions.

The quest for increased power and number of channels has pushed the payload system designers to look for more integration at component level.

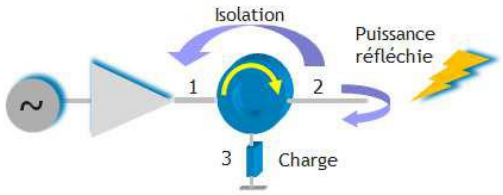


Figure 1 : Isolator applications

A preliminary synthesis of available SMD ferrite devices (isolators and circulators) that can be found in the market, with a selection of the small size and high frequency products. This review was done after performing a comprehensive analysis of available literature and patents [1][2][3][4][5] with a focus on the requirements of this project.

The analysis of these various SMD solutions shows that four distinct approaches exist as follows:

- Modification of the well-established drop-in technology by bending the strip leads or adding vertical leads to have all I/Os and ground on the same plane
- Modification of the microstrip technology by providing via holes or castellations to have all I/Os and ground on the same plane. - Integration of the ferrite device in a low cost plastic overmolded leadframe
- Design of a specific package with matched RF feedthroughs.

Main benefits and limitations of these approaches are shown in *Table* 1.

SMD solutions	Modified drop-in	Microstrip	Organic SMD	Specific SMD
SMD interface	Bended leads	Castellations	Leadframe or PCB	Matched RF feedthroughs
Advantages	Qualified technology Stress relief	High frequency Integration Reliability	Low cost	High frequency Stress relief EMC performance Miniaturization
Limitations	EMC performance Frequency capability Size	EMC performance No stress relief	EMC performance Frequency capability Reliability	Cost

Table 1 : Benefits and limitations of various SMD solutions

For COBHAM MICROWAVE, the best approach to design a hi-rel, high frequency SMD isolator suitable for space applications, is to develop a new SMD isolator technology rather than trying to adapt existing technologies and cope with their inherent limitations.

The technology concept developed by COBHAM MICROWAVE is presented in Figure 2. It is based on the stripline design of the isolator core, since it combines the advantages of compactness, lower losses, and EM interference immunity (compared to microstrip design). This core is packaged in a specific metal case to ensure electrical and magnetic shielding, and to close the magnetic path.

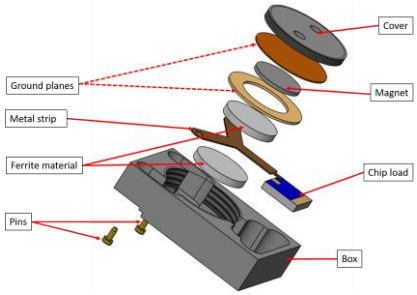


Figure 2 : Technology concept of SMD

II. DESIGN AND DEVELOPMENT

A. *Initial Objective*

The electrical parameters and specifications such as Insertion Loss, Return Loss and Isolation, specified in Table 2, are fully consistent with the needs in this frequency band. As these parameters are very dependent of the PCB used for SMD assembly, a great care shall be taken to design the test-jig.

Parameter	Units	Min	Max	Comment
Operating Frequency Range	GHz	17.7	20.2	
Insertion Loss	dB		0.5	Over Operating Frequency range
Return Loss	dB	19		
Isolation	dB	19		
Power Handling Average (forward) Average (reverse)	W	 1 0.5		
SE	dB	70		
Temperature Range Operating Non-Operating	°C	 -30 -40	 85 115	
Mechanical Environment Sine Vibration Random Vibration Shock		Minimum levels according to RD 3.		Shall cover all major platforms.
Radiation	Mrad	TBC		
Mass	g		2	
Envelope	mm³		13X10X4	
Interface				SMD ports Footprints to be provided.

Table 2 : Electrical parameters and specifications

The average power handling requirement is 1W in forward and 0.5W in reverse in 17.7 to 20.2 GHz. This corresponds to the low power classification as defined in ESCC3202 specification for ferrite isolators and circulators in Ka-band. Low power rating implies limited concerns in terms of self-heating, thermal management, and other high power phenomena such as Corona and Multipactor effects.

The most critical parameter of the specification is EMC shielding efficiency (SE) level. It should be noted that the measurement and the verification of the SE level shall be done on an unit mounted and soldered on a PCB.

In addition, the isolator shall be designed and customized to match with the final customer PCB.

Miniaturization and higher integration mean significant size and weight reduction compared to other isolator technologies like drop-in or coaxial. It also implies a benefit of being mounted and integrated close to other SMD components on the same PCB.

B. *RF Simulation*

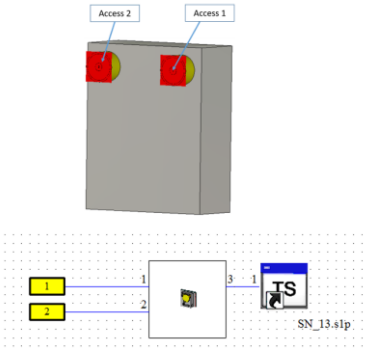


Figure 3 : Simulation model of the SMD isolator

Important mass-market devices - from computers, mobile communications devices and networks to satellites - depend on performant electromagnetic transmit and receive equipment. The design of electromagnetic systems requires an accurate modeling of electromagnetic fields.

Therefore, over the past decade, full-wave 3D EM simulators have become essential tools to design modern RF systems.

Designing this complex unit requires an accurate modeling tool. The full-wave 3D EM simulator CST is suitable to simulate it. Therefore, CST Microwave Studio with its time domain solver was used to design the isolator structure. Figure 3 shows the isolator design based on the Finite Integral Technique (FIT).

This electromagnetic (EM) software integrates Polder's model [6] that allow predicting permeability spectra of magnetized ferrites (M_s), internal field (h_{int}), and magnetic losses (ΔH).

Ferrites are magnetically biased and magnetic field is considered homogeneous. The preliminary simulation does not take into account the performance of the PCB.

Due to the power-handling requirement of 5W, a specific BeO chip load design was implemented.

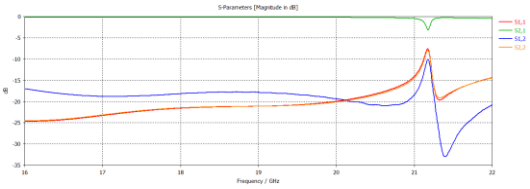


Figure 4 : RF simulation results

The preliminary simulation (Figure *4*) show a minimum Isolation of 17.5 dB versus 19 dB specified, and minimum return losses of 19 dB versus 19 dB specified.

These performances are both promising and encouraging. In addition, the simulation shows that the specified dimensions are achievable and that electrical performance is close to requested specifications.

Optimization of the stripline will be necessary to reach the specifications in the whole band.

C. *Prototypes and measurements*

Various iterations were performed on the prototypes and on the shape of the stripline in order to improve RF performance. Several prototypes (Figure *5*) were manufactured and characterized to validate all specifications and show a good repeatability.

The final stripline shape allowed to obtain compliant VSWR on port 1 and 2, and to avoid any further tuning. Tuning shall only be performed on the loaded port to improve Isolation value. Consequently, material consumption and workmanship are lowered.

Isolator prototypes were measured with a Vector Network Analyzer in 15-25 GHz. Thru-Reflect-Line (TRL) calibration procedure was performed in order to shift the reference plane of the test jig.

Figure 5 : Isolator Prototype

Figure 6 presents the measured S-parameters of one of the several manufactured prototypes of the Ka-band low power SMD isolator. These results confirm the full achievement of the expected RF performance, and the results distribution show confidence to secure future manufacturing margins.

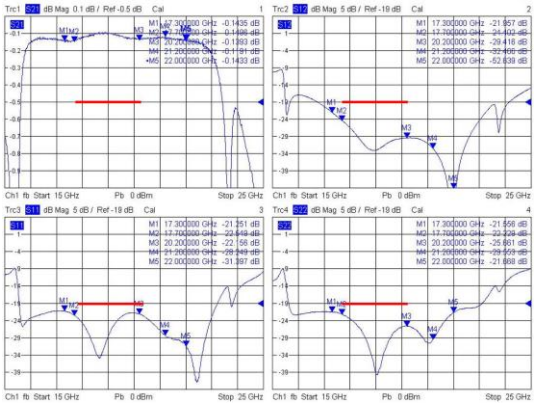


Figure 6 : Measurement results

To correctly perform a complete retro-simulation, it is necessary to integrate the resistive chip load in the simulation.

A highly dense mesh in the body of the load was used in order to simulate correctly the product. However, as a dense mesh greatly increases simulation time, a new technique has been used. It first defines a waveguide port between the end of the stripline and the load part. Secondly, it is requires to measure the load to be used in the component, and to connect the measurement result in S1P format to the simulated waveguide port.

The simulated structure is representative of the final prototype with identical dimensions for all its components (strip, ferrite, load, ground planes, etc ...).

The magnets and the magnetic circuit elements are not taken into account in the simulations. The ferrites are considered magnetically biased and the magnetic field homogeneous.

Retro-simulations using CST Microwave Studio were performed. A good correlation between measurements and simulations was achieved with the parameters listed in Table 2 (Figure 7).

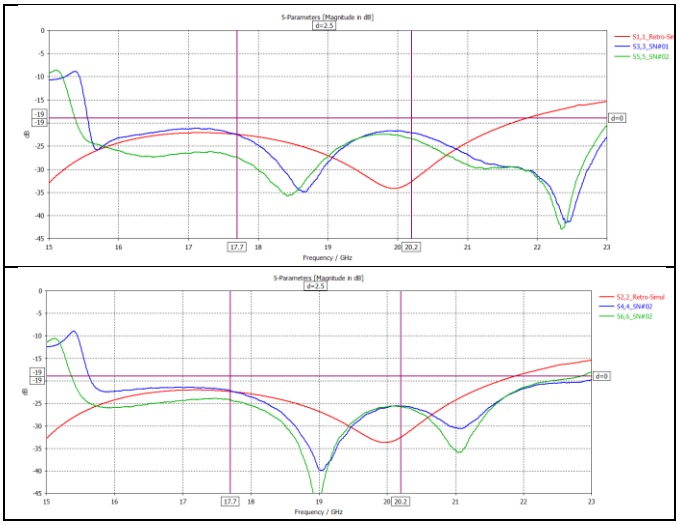


Figure 7 : Measured and simulated S-Parameters of ka-band low power SMD isolator

The test results present full compliance RF parameters in the extended functional frequency band 17.3 – 22 GHz.

D. *EMC measurement:*

One prototype was soldered on the test PCB to perform EMC test. A preliminary S-parameter test is performed to confirm good connection between isolator and PCB.

EMC test is performed at COBHAM in accordance with ESA ESCC Basic Specification No 24500: Reduced EMC Test Method for Radiated Emission and Radiated Susceptibility.

The measurements are performed with a CEM probe sniff around the part, and at a distance of 10 cm. The worst case measurement is recorded.

The shielding efficiency is calculated as follows:

	RF generator		Spectrum analyser			
S/N :	P_G (dBm) =	I_LIN (dBm)=	I_LOUT$_{(dBm)}$=	P_S (dBm) =	$G_{(dB)}$=	F $_{(Mhz)}$=	Se (dBi)=
Proto SN07	11	4,3	3,5	-103,43	6,26	19000	74,87

Distance = 10 cm : Se (dBi) = PG – PS + G – 20 log F(Mhz) + 47.56 - ILIN - ILOUT

Figure 8 : EMC measurement results

This result demonstrates the compliance of the shielding efficiency with the project specification (70 dBi).

III. MANUFACTURING AND EVALUATION OF TEST VEHICLES

A. *Manufacturing of test vehicles*

20 test vehicles tests of Ka-band low power SMD isolator have been manufactured according to the Process Identification Document and initially screened follow ESA Standards 3202,

all compliant with the specifications.

Figure 9 : Test vehicles

B. Evaluation of test vehicles

This section presents the evaluation test results according to the sequence of the ETP.

Group	Control	2A1	2A2	2B	2C	3	Spare
S/N	SN118	SN101 SN107 SN111 SN119	SN103 SN108 SN112 SN116	SN100 SN105 SN110	SN109 SN113 SN117	SN102 SN106 SN115	SN104 SN114

Table 3 : Allocation of evaluation units

1) Group 2 - Destructive tests

Subgroup 2A1 – Temperatures Step stress tests (4 units)

The desired power is delivered to each isolator at port 2 (reverse mode with port 1 being loaded). The power level is controlled by the input level of the signal generator (at 18 GHz), amplified by the power amplifier, monitored by the spectrum analyzer through a coupler, and splitted to the 4 isolators by a power divider. The power of 0.5W is verified by the power meter with a power probe connected at each output of the divider before connecting each of the DUTs. Ambient temperature close to the isolators is monitored by a thermocouple. Results are presented in Table *4*.

$P_{reverse}$ 0.5W		SN 101	SN 107	SN 111	SN 11
1st step: 85°C	Failure	0	0	0	0
2nd step: 115°C	Failure	0	0	0	0
3rd step: 145°C	Failure	0	0	0	0
4th step: 175°C	Failure	0	0	0	0

Table 4 : Temperatures Step stress tests results

Subgroup 2A2 – Reverse power step stress (4 units)

Self-heating was monitored by a thermocouple soldered on the isolator package, as close as possible to the load.
The test shall be performed according to the Evaluation Test Programme at 85°C (max operating temperature). Electrical measurements are performed after each step at room temperature in accordance with detail specification. Starting power shall be 0.5 W in reverse (max rated continuous power for isolator) applied at 18 GHz, the other port being short circuited and power steps shall be as shown in Table 5 .

T = 85°C		SN 103	SN 108	SN 112	SN 116
1st step: 0.5W 2 hours	Temperature (°C)	85	85	85	85
	Failure	0	0	0	0
2nd step: 1W 2 hours	Load Temperature (°C)	87	88	88	87
	Failure	0	0	0	0
3rd step: 1.5W 2 hours	Load Temperature (°C)	89	89	90	90
	Failure	0	0	0	0
4th step: 2W 2 hours	Load Temperature (°C)	90	90	91	92
	Failure	0	0	0	0
5th step: 2.5W 2 hours	Load Temperature (°C)	92	92	92	93
	Failure	0	0	0	0
6th step: 3W 2 hours	Load Temperature (°C)	93	93	93	95
	Failure	0	0	0	0
7th step: 3.5W 2 hours	Load Temperature (°C)	95	97	95	96
	Failure	0	0	0	0
8th step: 4W 2 hours	Load Temperature (°C)	98	98	97	97
	Failure	0	0	0	0
9th step: 4.5W 2 hours	Load Temperature (°C)	102	103	101	101
	Failure	0	0	0	drift

Table 5 : Reverse power step stress results

Slight drift is observed on this unit (SN0116) only after 4.5W but the part remain compliant. Power step stress tests completed (3 parts, up to 4.5 W each) with no failure, no drift.
One part, no failure, no drift up to 4W, but at 4.5W the SN0116 drift only on S22 with no degradation for the S21, S11 and S12 parameters. A destructive analysis has been carried out on this part.

Subgroup 2B – Vibration, Shock and Thermal stability tests (3 units)

Vibration test

Vibration step stress has been performed as:
- 4 Steps: 50g RMS + 50g RMS + 80g RMS + 100g RMS
- Duration for each step: 180 s x 3 axes

In order to reach the high RMS level specified, a trampoline, which amplifies acceleration amplitude levels, is used. Due to the small size and rigid nature of the unit without any resonance frequency below 2000 Hz, only the overall Grms level is important, whatever the density spectrum shape is. S parameter measurement and visual inspection showed no failure after all steps.

		SN 100	SN 105	SN 110
1st step: 50 g RMS	Failure	0	0	0
2nd step: 50 g RMS	Failure	0	0	0
3rd step: 80 g RMS	Failure	0	0	0
4th step: 100 g RMS	Failure	0	0	0

Table 6 : Vibration test results

Shock test

Subsequent to vibration step stress, shock step stress was performed as:
- Half sine 0,3 ms
- 3 Steps: 1500 g + 2000 g + 3000 g + 4000 g
- Number of shocks at each step : 18 (3 x 2 directions x 3axis)

Based on the S parameter measurement at room temperature after each step and visual inspection after each step, no anomaly was found and no failure was detected after the 3 steps.

		SN100	SN105	SN110
1st step: 1500 g	Failure	0	0	0
2nd step: 2000 g	Failure	0	0	0
3rd step: 3000 g	Failure	0	0	0
4th step: 4000 g	Failure	0	0	0

Table 7 : Shock test results

Subgroup 2C : Thermal cycling tests

Thermal cycling test has been planned as:

- Rapid change of temperature (two chamber method)
- 500 cycles -55/+125°C.
- Interim electrical measurements of the S parameters are performed after 50, 100, and 200 cycles at room temperature.
- Storage time: 15 min

Based on the S parameter measurement at room temperature after each step and visual inspection after each step, no failure was detected after any of the thermal cycle test steps.

		SN109	SN113	SN117
1st step: 50 cycles total	Failure	0	0	0
2nd step: 100 cycles total (+50)	Failure	0	0	0
3rd step: 200 cycles total (+100)	Failure	0	0	0
4th step: 500 cycles total (+300)	Failure	0	0	0

Table 8 : Thermal cycling test results

2) Group 3 : Accelerated Electrical Endurance

It has been agreed with ESA to perform this accelerated electrical endurance test by a temperature storage at the 0W temperature according to the derating curve. The 5W Diconex chip load derates linearly from max power at 110°C to 0W at 150°C. So the 3 units have been subjected to a temperature storage in a climatic chamber 1000h@150°C.

The following table show the measurements of the 3 units performed after storage at 150°C at interim points after 168h, 500h and 1000h.

		SN102	SN106	SN115
1st step: after 168h	Failure	0	0	0
2nd step: after 500h (+332h)	Failure	0	0	0
3rd step: after 1000h (+500h)	Failure	0	0	0

Table 9 : Temperature storage in climatic chamber results

IV. Development, Manufacturing and Evaluation of New Test Vehicles

A. Development

Two others configurations have been developed.

The first one is designed with a 10W chip load, this configuration is based on the last version (5W chip load). The main changes are the ferrite material, the chip load and the metal stripline.

In order to study correctly this product, it is necessary to integrate the load in the simulation to take into account the behaviour of the load.

The measurement results of the 10W-18GHz chip load show a limitation in the frequency range. This load can be used up to 20 GHz.

The simulation results obtained confirm that the functional band of the chip load is up to 20.2 GHz. With the preliminary simulation, isolation is calculated at 17.5 dB minimum for 19 dB specified and return losses are calculated at 23 dB minimum for 19 dB specified. These preliminary results obtained in simulation are both promising and encouraging. Modifications the shape of the metal stripline has been necessary in order to achieve the requested electrical performance in the whole band.

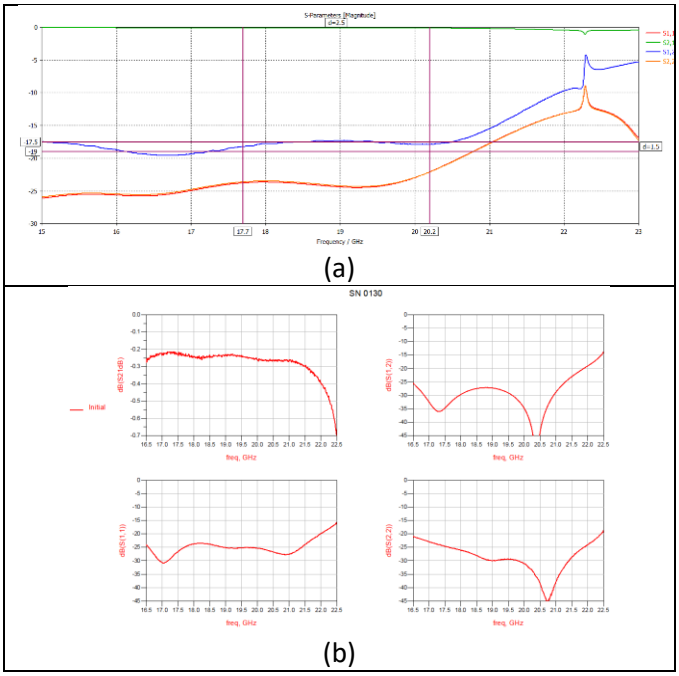


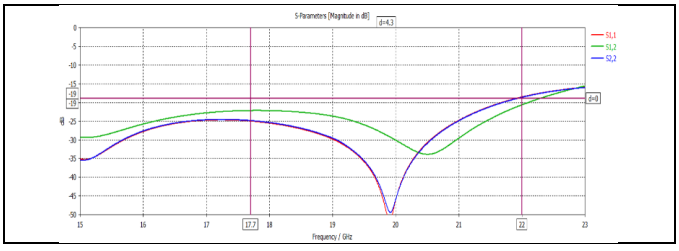
Figure 10 : Simulated (a) and measured (b) S-Parameters of ka-band SMD isolator Version V1 (10W chip load)

The 10 W chip load is developed up to 18 GHz, for this activity Cobham, with technical cleverness by modifying the stripline shape on load side and few tuning, succeeded to make operate this load up to 21.3 GHz. The obtained measurement results present full compliance RF parameters in the functional frequency band 17.3 – 21.3 GHz.

The second one is designed with an integrated load that the stripline is stacked between two-absorber loads. This version is based on the 5W chip load. The main changes are the internal shape of the box, the load and the metal stripline.

In order to study correctly this product, it is necessary to integrate the Absorber load in the simulation to take into account the behaviour of the load. Access 1 & 2 are connected with 50 ohms. Access 3, the strip-line is placed between two MF absorber materials. Indeed, to integrate this load in the simulation it was necessary to use a highly densified mesh in the body of the load in order to simulate correctly the product.

Simulation results for Isolation is 19 dB minimum for 19 dB specified and return losses are calculated at 19 dB minimum for 19 dB specified. These preliminary results are both promising and encouraging. Modifications the shape of the metal stripline will be necessary in order to achieve the requested electrical performance in the whole band.



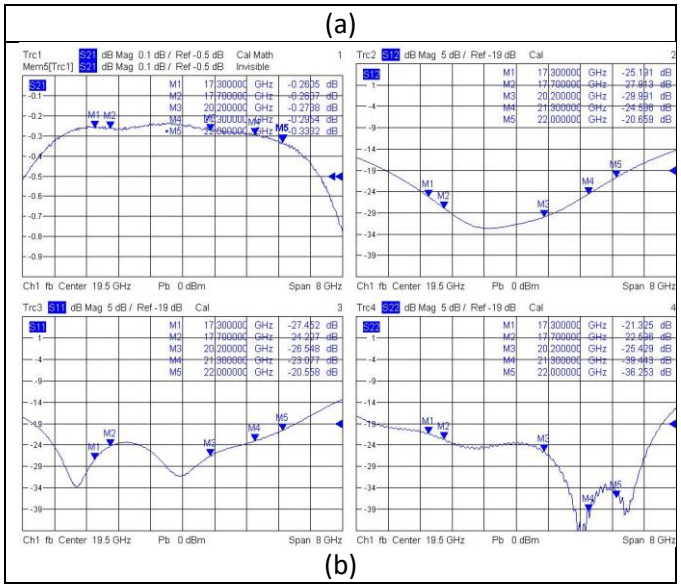


Figure 11 : Simulated (a) and measured (b) S-Parameters of ka-band SMD isolator Version V2 (Absorber load)

The obtained measurement results present full compliance RF parameters in the functional frequency band 17.3 – 22 GHz.

B. *Manufactured and Evaluation*

Six evaluation samples of each versions have been manufactured and screened. No noticeable degradation of the performances is found on the screened parts. Measurement results of all the units present full-compliance RF parameters in temperatures range.

1) *10W chip load version*

Group	Control	2A2	Spare
S/N	SN134	SN130 SN131 SN131 SN133	SN135

Table 10 : Allocation of evaluation units

Subgroup 2A2 – Reverse power step stress (4 units)

T = 85°C		SN 130	SN 131	SN 132	SN 133
1st step: 4 W	Temperature (°C)	92	92	92	92
2 hours	Failure	0	0	0	0
2nd step: 5 W	Load Temperature (°C)	95	95	94	96
2 hours	Failure	0	0	0	0
3rd step: 6 W	Load Temperature (°C)	97	97	98	98
2 hours	Failure	0	0	0	0
4th step: 7 W	Load Temperature (°C)	100	98	99	100
2 hours	Failure	0	0	0	0
5th step: 8 W	Load Temperature (°C)	104	102	101	103
2 hours	Failure	0	0	0	0
6th step: 9 W	Load Temperature (°C)	106	108	104	106
2 hours	Failure	0	0	0	0

Table 11 : Reverse power step stress results (10W chip load version)

All power stress steps test were completed. No drift, no failure were found on the parts. No RF degradation was detected after each Power step.

2) *Absorber load version*

Group	Control	2A2	Spare
S/N	SN150	SN151 SN152 SN153 SN154	SN155

Table 12 : Allocation of evaluation units

Subgroup 2A2 – Reverse power step stress (4 units)

T = 85°C		SN 151	SN 152	SN 153	SN 154
1st step: 0.5 W	Temperature (°C)	87	87	87	87
2 hours	Failure	0	0	0	0
2nd step: 1 W	Load Temperature (°C)	91	90	90	92
2 hours	Failure	0	0	0	0
3rd step: 1.5 W	Load Temperature (°C)	96	94	94	96
2 hours	Failure	0	0	0	0
4th step: 2 W	Load Temperature (°C)	101	99	99	102
2 hours	Failure	0	0	0	0
5th step: 2.5 W	Load Temperature (°C)	107	104	105	109
2 hours	Failure	0	0	0	drift

Table 13 : Reverse power step stress results (Absorber load version)

Power step stress tests completed (3 parts, up to 2.5 W each) with no failure, no drift. One part, no failure, no drift up to 2 W, but at 2.5W the SN01154 drift only on S12 with no degradation for the S21, S11 and S22 parameters. Although the temperature of the box (top side) was not very high, it was noticed a degradation of the isolation parameter.

V. CONCLUSION

This activity permitted to design, manufacture, and test an SMD Ka-band isolator (V0 5W chip load).

In addition, Cobham extended and completed the study on two other variants: a very low power (V2 absorber load), and a high power (V1 10W chip load). All models passed ESCC Evaluation tests. Moreover, initial specifications were improved on frequency band and insertion loss parameters (Table 14). Cobham considers this activity successful.

Parameters	Spec ESA	Version V0 (chip load 5W)	Version V1 (chip load 10W)	Version V2 Absorber load (0.5W)
Frequency band	17.7 – 20.2 GHz	17.3 – 22 GHz	17.3 – 21.3 GHz	17.3 – 22 GHz
Reverse power	0.5 W	2 W	6 W	0.5 W
Envelope	13 x 10 x 4 mm^3	10.45 x 8.45 x 4 mm^3	10.45 x 8.45 x 4 mm^3	10.45 x 8.45 x 4 mm^3
Insertion losses	0.5 dB	0.4 dB	0.4 dB	0.4 dB

Table 14 : Proposed Specifications

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